REMARKS

In an Office Action mailed on October 9, 2003, claims 1, 3-5, 8, 9, 11, 13, 18, 20-22 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Olarig; claims 2, 7, 10, 12, 16-17, 19 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of alleged Applicant's Admitted Prior Art (AAPA); and claims 6, 14, 27 and 28 were objected to as being dependent upon rejected base claims but allowable if rewritten in independent form. These rejections are discussed below.

In the latest Office Action, the Examiner contends that, "the Applicant fails to credit the artisan with any skill at all." Final Office Action, 3. However, contrary to the Examiner's statement, Applicant is not discrediting the level of skill in the art, but rather, Applicant is requiring the Examiner to show where the prior art contains the alleged suggestion or motivation to modify Chen to derive the missing claim limitations. The Examiner, having knowledge of the invention, is contending that the modifications to Chen would have been obvious to one of skill in the art. This is not, however, the test for obviousness. Rather, a *prima facie* case of obviousness requires the Examiner to show the existence of a suggestion or motivation in the art for the modification, without knowledge of the claimed invention. The Examiner has failed to satisfy this component.

The Examiner has now added Olarig to the § 103 rejections. Olarig states that because the bus 204 is closer to the microprocessor and memory than the bus 208, transactions happen faster between the microprocessor and memory over the bus 204. This is apparent, in view of Figure 3, as transactions over the bus 204 must propagate through a bridge 202, where transactions over the bus 208 must propagate through the bridge 206 as well as the bridge 202. However, in the claimed invention, the buffer is located closer to one bus than to another bus. The bus distances, however, do not change. In short, neither Olarig nor any of the other references cited by the Examiner teaches or suggests a buffer that is adapted to capture data directly from a memory bus and is located closer to a local bus than to a memory bus. Without a showing where the prior art teaches or suggests such a modification of Chen, the Examiner has failed to establish a *prima facie* case of obviousness of independent claims 1, 11 and 18. The

Examiner still fails to address the limitations of claim 22, i.e., extending a memory bus into a bridge.

Dependent claims 2-10, 12-17, 19-21, 23 and 26-28 are patentable for at least the reason that these claims depend from allowable independent claims. Thus, in view of the foregoing, reconsideration and withdrawal of the § 103 rejections of claims 1-23 and 26-28 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the § 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (MCT.0078US).

Respectfully submitted,

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